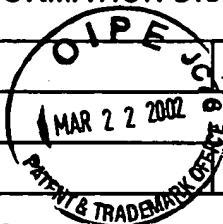


## INFORMATION DISCLOSURE CITATION

Atty. Docket No.	04284.0856	Serial No.	10/051,280
Applicant	Atsushi SHIMBO		
Filing Date	January 22, 2002	Group:	Not Yet Assigned <u>2124</u>



## U.S. PATENT DOCUMENTS

Examiner Initial*	Document Number	Issue Date	Name	Class	Sub Class	Filing Date If Appropriate

## FOREIGN PATENT DOCUMENTS

Document Number	Publication Date	Country	Class	Sub Class	Translation Yes or No

## OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

CD	S. KAWAMURA et al., "COX-ROWER ARCHITECTURE FOR FAST PARALLEL MONTGOMERY MULTIPLICATION", Eurocrypt 2000, LNCS 1807, pp. 523-538, 2000.
CD	K. POSCH et al., "MODULO REDUCTION IN RESIDUE NUMBER SYSTEMS", IEEE Transactions on Parallel and Distributed Systems, Vol. 6, No. 5, pp. 449-454, May 1995.

Examiner:	Date Considered: <u>11/10/04</u>
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Atty. Docket No.	4284.0856	Appln. No.	10/051,280
Applicant	Shimbo		
Filing Date	January 22, 2002	Group:	2121-2124

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Examiner Initial*	Document Number	Issue Date	Name	Class	Sub Class	Filing Date If Appropriate

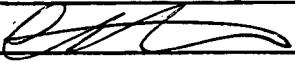
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Document Number	Publication Date	Country	Class	Sub Class	Translation Yes or N

## OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

CD	U.S. Patent Application Serial No. 09/699,481, filed October 31, 2000, to Kawamura

Examiner: 	Date Considered: 11/10/04
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